



## Processor

TMS320C62x Series

## Technology

ITU-T G.728 is low delay speech coder standard, for compressing toll quality speech (8000 samples/second). G.728 Annex G (G.728 G) is a fixed point specification of the coder working at a bit rate of 16000 bits/second. G.728 Annex I (G.728 I) is the packet loss concealment (PLC) technique used along with G.728 G. G.728 Annex H is the specification of the coder working at bit rate of 12800 bits/second and 9600 bits/second. G.728 coders are widely used for applications that require very low algorithmic delay. The typical application of this speech coder is in telephony over packet networks, especially voice over cable and VoIP. This is a very robust speech coder, with very good speech quality, comparable to 32 kbit/s ADPCM.

G.728 coders are based on the principle of Low Delay-Code Excited Linear Prediction (LD-CELP). This coder has the conventional approach of analysis-by-synthesis for fixed codebook search, which is generally available in all CELP class coders. The low algorithmic delay of the coder is achieved using backward adaptation of predictors and gain. Though the algorithmic delay can be as low as 0.625 msec (5 samples), the frame size of the coder is 2.5 msec (20 samples).

## Features

- Fully compatible/bit-exact with the following standards
  - *ITU-T G.728 (09/92)*  
Coding of speech at 16 kbit/s using Low Delay Code Excited Linear Prediction
  - *ITU-T G.728 Annex G (11/94)*  
16 kbit/s fixed point specification
  - *ITU-T G.728 Annex G Corrigendum 1 (02/00)*  
16 kbit/s fixed point specification
  - *ITU-T G.728 Annex I (05/99)*  
Frame or packet loss concealment for the LD-CELP decoder
  - *ITU-T G.728 Annex H (05/99)*  
Variable bit-rate LD-CELP operation mainly for DCME at rates less than 16 kbit/s.
- The implementation is verified with the following standard
  - *ITU-T G.728 Appendix 1 Verification tools (07/95)*  
Programs and test sequences for implementation verification of the algorithm of the G.728 16 kbit/s LD-CELP speech coder.
- Texas Instruments eXpressDSP™ compatible software architecture.
- Little endian implementation (If required it can be converted to big endian)
- Frame based design. Frame is 20 samples (2.5 msec).
- Packet loss concealment (PLC) is activated in G.728 I. If PLC is not required, it can be disabled. When PLC is deactivated decoder will work identical to G.728 G.
- The enabling/disabling of post filter in decoder is selectable at the time of decoder channel initialization.
- Full duplex multi-channel capability.
- Flexible interface with 'C' callability, with a single archive file for all functions.
- Relocatable program and data spaces. Static (state) and scratch data memory are dynamically relocatable. Program and table data spaces can be fragmented.

- The code is interruptible and full re-entrant. This code can be used in systems with multi threaded software architecture.

## Performance

### Resource Requirements

(Internal Code Version 1.4, CCS Version 2.21)

### Memory (KBytes)

Program Memory	Data Memory		
	Tables	Static/Channel	Scratch
51.936	5.050	4.196	1.912

### MCPS

MCPS measurements are taken on **TMS320C6202** based EVM target platform, with all memory requirements placed internal.

Function	MCPS					
	16kbps		12.8kbps		9.6kbps	
Encoder	14.83		13.13		12.19	
Decoder	Postfilter enable	Postfilter disable	Postfilter enable	Postfilter disable	Postfilter enable	Postfilter disable
	11.23	10.46	11.20	10.42	11.24	10.46
Full Duplex	26.06	25.29	24.33	23.55	23.43	22.65

### Availability

Now.

For further information please visit our web site, <http://www.ncoretech.com> or email to: [ip@ncoretech.com](mailto:ip@ncoretech.com) or contact:

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