



Encore's G.723.1

Technology

This coder has two bit rates, 5.3 and 6.3 Kbps. Both bit rates share the same short-term analysis techniques for processing the speech. For long-term analysis of speech, the algorithms used are different. For 5.3 Kbps coder, Algebraic Code Excited Linear Prediction (ACELP) principles are used where as in 6.3 Kbps coder, Multi Pulse-Maximum Likelihood Quantization (MP-MLQ) techniques are used.

The coder works on a frame of 240 speech samples (30 msec). Besides, there is a look ahead of 60 samples (7.5 msec). So the total algorithmic delay for the coder is 37.5 msec.

Features

- Fully compatible/bit-exact with the ITU-T G.723.1 standard with Annex A, version 5.1, with discontinuous transmission (DTX) support, using Voice Activity Detection (VAD) and Comfort Noise Generation (CNG).
- Works in little endian mode. The system should be configured for little endian mode.
- Front-end high pass filter in encoder and post filter in decoder can be enabled or disabled at the time of channel initialization.
- Coder bit rate selection (6.3 or 5.3 Kbps) and DTX (VAD/CNG) enabling or disabling can be done on a frame basis.
- Full duplex multi-channel capability.
- Flexible interface with 'C' callability, with a single archive file for all functions.
- Built-in scratch memory management to avoid run-time overloading of system stack memory.
- Relocatable program and data spaces. Static (state) and scratch data spaces are dynamically relocatable. Program and table data spaces can be fragmented.
- The code is interruptible and re-entrant. It can be used in systems with multi threaded software architecture.

Platforms

- TMS320C64X
- TMS320C62X
- TMS320C54X
- TMS320C55X
- ARM9E
- Coldfire (MCF52xx,53xx,522xx)
- PowerPC

Performance Numbers

Platform	Program Memory (KBytes)	Data Memory (KBytes)			MIPS
		Static/Channel	Scratch	Tables	
TMS320C64X	80.09	2.8	4.9	19.44	7.72
TMS320C62X	75.69	2.8	4.9	19.44	11.78
TMS320C54X	21.72	1.76	2.8	19.4	16.64
TMS320C55X	19.72	1.76	2.8	19.4	12.39
ARM9E	42.0	1.76	2.8	19.4	*39.0
M52xx, M53xx, M522xx	36	1.74	2.58	18.51	46.8
PowerPC					

* This cycle was measured with 0 wait state memory, 16 Kbytes I/D cache, 32 bit bus width, ratio of core clock to bus clock=1

Availability

Now.

For further information please visit our web site, <http://www.ncoretech.com> or email to: jp@ncoretech.com

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