



Encore's GSM-AMR-NB

Technology

GSM-AMR is an Adaptive Multi Rate (AMR) speech coder standard introduced by the 3rd Generation Partnership Project (3GPP), which is a partnership project of various standards organizations, for compressing the toll quality speech (8000 samples/second). This speech coder is mainly used for speech compression in the 3rd generation mobile telephony.

This codec has eight basic bit rates, 12.2, 10.2, 7.95, 7.40, 6.70, 5.90, 5.15 and 4.75 Kbit/s. This codec works on the principle of Algebraic Code Excited Linear Prediction (ACELP) for all bit rates. To reduce average bit rate, this codec supports the discontinuous transmission (DTX), using Voice Activity Detection (VAD) and Comfort Noise Generation (CNG) algorithms. There are two types of VAD algorithms.

The coder works on a frame of 160 speech samples (20 msec), and no look ahead is required. So the algorithmic delay for the coder is 20 msec.

Features

- Fully compatible with the following 3GPP GSM-AMR standards

3GPP TS 26.071 V4.0.0	AMR Speech Codec; General Description
3GPP TS 26.090 V4.0.0	AMR Speech Codec; Transcoding functions
3GPP TS 26.091 V4.0.0	AMR Speech Codec; Error concealment of lost frames
3GPP TS 26.092 V4.0.0	AMR Speech Codec; Comfort noise aspects
3GPP TS 26.093 V4.0.0	AMR Speech Codec; Source controlled rate operation
3GPP TS 26.094 V4.0.0	AMR Speech Codec; Voice activity detector

Fully bit exact with the following 3GPP GSM-AMR standard reference code

3GPP TS 26.071 V4.0.0	ANSI-C code for AMR speech codec (Code Version 7.6.0)
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Fully tested using the test vectors given in the following 3GPP GSM-AMR standard

3GPP TS 26.074 V4.0.0	AMR Speech Codec; Test sequences
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- Coder bit rate selection (any of the 8 rates) and DTX (VAD/CNG) enabling or disabling can be done on a frame basis.
- Selection of VAD options (NO_VAD, VAD1 or VAD2) at the time of initialization.
- Full duplex multi-channel capability.
- Flexible interface with 'C' callability, with a single archive file for all functions.
- Built-in scratch memory management to avoid run-time overloading of system stack memory.
- The code is interruptible and frame re-entrant. It can be used in systems with multi threaded software architecture.

Platforms

- TMS320C64X
- TMS320C62X
- TMS320C54X
- TMS320C55X
- ARM9E
- COLDFIRE

Performance Numbers

Platform	Program Memory (KBytes)	Data Memory (KBytes)			MIPS
		Static/Channel	Scratch	Tables	
TMS320C64X	148.22	3.07	6.05	34.26	10.0
TMS320C62X	140	3.07	6.05	34.26	11.8
TMS320C54X	51.48	3.07	6.05	34.26	19.28
TMS320C55X	55.4	3.07	6.05	34.26	19.34
ARM9E	89.2	3.07	6.05	34.26	*44.0

* This cycle was measured with 0 wait state memory, 16 Kbytes I/D cache, 32 bit bus width, ratio of core clock to bus clock=1

Availability

Now

For further information please visit our web site, <http://www.ncoretech.com> or email to: jp@ncoretech.com