



## Encore's AMR-WB

### Technology

The Adaptive Multi-Rate-Wideband Codec (AMR-WB) is a speech coder standard introduced by the 3<sup>rd</sup> Generation Partnership Project (3GPP), which is a partnership project of various standards organizations, for compressing the toll quality speech (16,000 samples/second). The AMR-WB Codec has been approved by the ITU-T standards body and is referred to as G.722.2. This speech coder is mainly used for speech compression in the 3rd generation mobile telephony.

This codec has nine basic bit rates, 23.85, 23.05, 19.85, 18.25, 15.85, 14.25, 12.65, 8.85 and 6.6 kbit/s. This codec works on the principle of Algebraic Code Excited Linear Prediction (ACELP) for all bit rates. To reduce average bit rate, this codec supports the discontinuous transmission (DTX), using Voice Activity Detection (VAD) and Comfort Noise Generation (CNG) algorithms.

The coder works on a frame of 320 speech samples (20 msec), and a look ahead of 5 msec is required. So the algorithmic delay for the coder is 25 msec.

### Features

- Fully compatible with the following 3GPP AMR-WB standards

3GPP TS 26.171 V5.0.0	AMR Wideband Speech Codec; General Description
3GPP TS 26.190 V5.0.0	AMR Wideband Speech Codec; Transcoding functions
3GPP TS 26.191 V5.0.0	AMR Wideband Speech Codec; Error concealment of lost frames
3GPP TS 26.192 V5.0.0	AMR Wideband Speech Codec; Comfort noise aspects
3GPP TS 26.193 V5.0.0	AMR Wideband Speech Codec; Source controlled rate operation
3GPP TS 26.194 V5.0.0	AMR Wideband Speech Codec; Voice activity detector

Fully bit exact with the following 3GPP GSM-AMR WB standard reference code

3GPP TS 26.173 V5.4.0	ANSI-C code for AMR Wideband speech codec (Code Version 5.4.0)
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Fully tested using the test vectors given in the following 3GPP GSM-AMR-WB standard

3GPP TS 26.174 V5.3.0	AMR Wideband Speech Codec; Test sequences
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- Coder bit rate selection (any of the 9 rates) and DTX (VAD/CNG) enabling or disabling can be done on a frame basis.
- Full duplex multi-channel capability.
- Flexible interface with 'C' callability, with a single archive file for all functions.
- Built-in scratch memory management to avoid run-time overloading of system stack memory.
- The code is interruptible and frame re-entrant. It can be used in systems with multi threaded software architecture.

### Platforms

- TMS320C64X
- TMS320C62X
- ZSP400
- ARM9E
- ARM11

## Performance Numbers

Platform	Program Memory (K Bytes)	Data Memory (K Bytes)			MIPS
		Static/Channel	Scratch	Tables	
TMS320C64X	108.56	4.54	9.58	31.88	25.0
TMS320C62X	147.56	4.54	9.58	31.88	30.0
ZSP400	49.12	4.32	8.6	31.88	34.4
ARM9E	88.65	4.54	9.58	31.88	*94.0
ARM11	134.0	4.28	9.58	31.88	**91.68

\* This cycle was measured with 0 wait state memory, 16 Kbytes I/D cache, 32 bit bus width, ratio of core clock to bus clock=1

\*\* This cycle was measured with 0 wait state memory, 8 Kbytes I/D cache, 32 bit bus width, ratio of core clock to bus clock=1 (MCCFG = 1)

## Availability

Now

For further information please visit our web site, <http://www.ncoretech.com> or email to: [ip@ncoretech.com](mailto:ip@ncoretech.com)

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