



# Encore's Acoustic Echo Canceller (AEC)

## Technology

The Encore's AEC algorithm is based on advanced adaptive filter algorithm with robust double talk detection, allowing convergence even while both parties are talking. This algorithm continually tracks changes in the echo path, regardless of double-talk, as long as a reference signal is available for the echo canceller. The AEC algorithm is also capable of handling non-linear harmonic distortion which would come from speaker path non-linearity

## Features

- Configurable echo tail length upto 256ms.
- Achieves up to 30dB of terminal coupling loss (TCLwst) by adaptive means, without inserting any attenuation
- Convergence rate > 30dB/sec
- Robust double talk detection.
- Faster convergence time.
- Adjustable gain pads at Sin and Sout to compensate for different system requirements.
- Capable of handling speaker non-linear harmonic distortion. AEC uses a (optional) post-processing technique, which is based on correlation between spectral amplitudes of residual echo and echo replica. It suppresses highly non-linear residual echo without any perceptual loss.
- Control of Non-Linear Processor thresholds for suppression of residual non-linear echo
- Optional Comfort Noise Generation (CNG). NLP/CNG, attenuates residual echo to background noise level or user configured level.
- High pass filters at Rin and Sin for removal of DC components in PCM channels
- Availability of tuning parameters to optimize the algorithm performance for a system.
- Multi-channel Capability.
- Flexible Programming Interface ('C' Callable).
- Provided in the form of Hardware Independent Library for easy pointing to the target platform.

## Platforms

- TMS320C64x
- TMS320C55x
- ZSP400 and ZSP200
- Coldfire (MCF52xx, 53xx, 522xx)

## Performance Numbers (For 64 msec tail length)

Platform	Program Memory (KBytes)	Data Memory (KBytes)			MIPS
		Static/Channel	Scratch	Tables	
TMS320C64X	42	6.4	3.75	0.6	14.9
TMS320C55X	3.2	6.78	3.2	3.28	18.5
ZSP400	8.75	6.78	3.2	3.28	19.05
ARM9E	25	6.78	3.2	3.28	*45.0
MCF52xx, 53xx, 522xx	10.5	8	1.7	3.44	50

- This cycle was measured with 0 wait state memory, 16 Kbytes I/D cache, 32 bit bus width, ratio of core clock to bus clock=1

## Availability

Now

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