



Encore's Packet Loss Concealment (PLC)

Technology

Packet Loss Concealment (PLC) algorithms, also known as frame erasure concealment algorithms, hide transmission losses in an audio system where the input signal is encoded and packetized at a transmitter, sent over a network, and received at a receiver that decodes the packet and plays out the output. Many of the standard CELP-based speech coders have PLC algorithms built into their standards. *Encore's* PLC provides a method for those codes which do not have in-built frame erasure concealment algorithm such as G.711, G.726, G.727 and G.722.

Features

- The PLC algorithm is compliant to G.711 Appendix I.
- Frame based design.
- Flexible interface with 'C' callability, with a single archive file for all functions.
- Relocatable program and data spaces. Static (state) and scratch data memory are dynamically relocatable. Program and table data spaces can be fragmented.
- The code is interruptible and frame re-entrant. This code can be used in systems with multi threaded software architecture.

Platforms

- TMS320C64X
- TMS320C62X
- TMS320C55X
- ARM9E
- ARM9
- PowerPC

Performance Numbers

Platform	Program Memory (K Bytes)	Data Memory (K Bytes)			MIPS
		Static/Channel	Scratch	Tables	
TMS320C64X	9.32	1.62	0.2	0.1	1.2
TMS320C62X	11	1.62	0.2	0.1	1.5
TMS320C55X	2.76	1.62	0.2	0.1	1.56
ARM9E	10	1.62	0.2	0.1	*3.4
Motorola PowerPC 8248	10	1.62	0.2	0.1	3.5

* This cycle was measured with 0 wait state memory, 16 Kbytes I/D cache, 32 bit bus width, ratio of core clock to bus clock=1

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